An adaptive frequency synthesizer architecture reducing reference sidebands

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Abstract—An adaptive phase-locked loop (PLL) frequency synthesizer architecture for reducing reference sidebands at the output of the frequency synthesizer is described. The architecture combines two tuning loops: one is the main loop for locking the PLL frequency synthesizer and operating all the time, the other one is auxiliary loop for reducing reference sidebands and operating only when the main loop is closely locked. A 1.8 V 1GHz fully integrated CMOS dual-loop frequency synthesizer is designed in a 0.18um CMOS process. The suppression of the reference sidebands of the proposed frequency synthesizer is 13.8dB more than that of the general frequency synthesizer.

I. INTRODUCTION

As the feature size of MOSFET processes shrink, the MOSFET sub-threshold drain-to-source leakage current when the transistor is supposedly turned off becomes increasingly large. In a phase-locked loop (PLL) frequency synthesizer, the charge pump (CP) may draw large enough leakage current when the CP is supposedly off to cause reference sidebands in the PLL’s output; the imperfection in the charge pump’s implementation can also generate reference sidebands in the PLL’s output [1,2]. The loop filter also draws leakage current whether it is implemented in active or passive devices or not.

In frequency synthesizer, this increased leakage current may no longer be ignored. Therefore, there is a need in the art for improved frequency synthesizer architecture that is fabricated using small feature-sized MOSFET processes.

II. THE ARCHITECTURE AND THE THEORY OF OPERATION OF THE PROPOSED FREQUENCY SYNTHESIZER

A. Architecture

The general architecture and the operation theory of the frequency synthesizer are discussed in detail in some literatures [3,4]. Fref is defined as the reference frequency, Fbak is defined as the frequency of VCO’s output after dividing N. The output frequency of the VCO (Fout) is equal to N • Fref if the PLL is locked. Also, the CP will charge current to LPF when UP signal is logic high, and discharge current when DN signal is logic high, vice versa.

The architecture of the proposed frequency synthesizer is shown in figure 1. The architecture includes two loops: the first (or main) loop is consisted of phase-frequency detector (PFD), CP, low-pass filter (LPF), voltage-controlled oscillator (VCO) and N divider (/N); the other phase-frequency detector (PFD2), two integrators, two voltage-controlled current sources (VCCSs) and the shared blocks including CP, LPF, VCO and N divider with the first loop form the second (or auxiliary) loop. The CP’s output (Icp) is not affected by the current outputs of the two VCCSs because the current outputs of the two VCCSs are added in CP’s output simply.

![Figure 1. The architecture of the proposed frequency synthesizer](image)

The first loop operates all the time for locking the phase-lock loop, and the second loop starts operating after the first loop has operated the defined time Td. The defined time Td is implemented by counting the reference frequency (Fref) using one counter, which is shown in figure 1. Here, Td is also defined as the locking time of PLL frequency synthesizer if only the main loop is used.
The PLL frequency synthesizer can normally locked the desired frequency if the second loop is disabled by the EN signal. The PFD2 is disabled while the EN signal is logic low, vice versa. If the EN signal is logic low, the two outputs of the PFD2 are all zeros, then the two outputs of the integrators are also zeros, finally, two outputs of the VCCSs are zeros.

Also, the second loop will have no effect on the whole system in figure 1 whether the PFD2 is enabled or not. If PFD2 is disabled, the outputs of PFD2 are zeros; If PFD2 is enabled, the second loop will also not pull or affect the first loop in figure 1 because the outputs of VCCSs are a little current only for compensation.

**B. Theory of operation**

The motivation of the proposed architecture is reducing reference sidebands. The method is that the leakage current from CP and LPF is compensated using the property of the PFD with or without dead zone. The dead zone property of the PFD is discussed in detail recently [5,6]. Generally, the frequency synthesizer uses the PFD without dead zone.

Here, the PFD in figure 1 is PFD without dead zone; The PFD2 in figure 1 is PFD with dead zone.

In PLL locked status, the output signals (UP and DN) of the LPF in figure 1 are shown in figure 2 while there is leakage current in CP and LPF if only one loop is used. The duration of $\Delta T$ in logic high of UP signal in figure 2 is used to compensating the leakage current in this condition. However, in ideal case, $\Delta T$ should be equal to 0 while there is no leakage current.

![Figure 2. the output of PFD without dead zone](image)

Also, if only one loop is used, the output signals (UP and DN) of the PFD with dead zone are shown in figure 3 while there is leakage current in CP and LPF in PLL locked status. Now, the duration in logic high of UP signal in figure 3 is also used to compensating the leakage current. However, the duration in logic high of UP signal should be also equal to 0 in ideal case while there is no leakage current.

However, there are serious reference sidebands at the output of the frequency synthesizer while there is leakage current from CP and LPF and only one loop is used.

In this paper, referring to figure 1, the outputs of the PFD2 are used to compensating the leakage current from CP and LPF because the status of the leakage current can be denoted distinctly from the two outputs of PFD2 while the PLL is closely locked. There are two statuses for the leakage current: the first is defined as the leakage current from the Vctrl node to ground; the second is defined as the leakage current from power supply to Vctrl node.

![Figure 3. the output of PFD with dead zone](image)

If the first case is true in PLL frequency synthesizer, the outputs of the PFD and PFD2 are shown in figure 2 and figure 3, respectively. Then, the outputs of the PFD2 are integrated respectively. Finally, the VCCSs convert the output voltages of integrators into currents in order to compensating the leakage current. It is an adaptive process because only one of the output voltages of the two integrators is larger than zero according to the status of the leakage current. As a result, the voltage of the Vctrl node will vary very small and keep closely constant. The reference sidebands at the output of the frequency synthesizer can be reduced significantly. That is to say, the leakage current can be compensated adaptively by the second loop in figure 1.

**III. CIRCUIT IMPLEMENTATION AND SIMULATION RESULTS**

![Figure 4. the transient voltage of the Vctrl node versus the locking time if only the main loop is used](image)

A 1.8V 1GHz fully integrated CMOS dual-loop frequency synthesizer is designed using a 0.18um CMOS process according to figure 1. Here, the integrators are implemented simply as two identical LPFs with passive resistors and capacitors respectively. And the VCCSs are implemented as active Gms. In this design, 1) $\text{Freq} = 1$MHz; 2) the gain of the VCO is equal to 60MHz; 3) introducing intentionally 800nA leakage current from the Vctrl node to
ground for emphasizing the effect of the leakage current on reference sidebands.

Figure 5. the enlarged partially of the figure 4

Figure 6. the output spectrum of the frequency synthesizer if only the main loop is used

If only the main loop is used, the voltage of the Vctrl node is shown in figure 4 when the PLL operates. Figure 5 is the enlarged partially of the figure 4. Figure 6 is the output spectrum of the frequency synthesizer. From figure 4-6, we can find that the voltage variation of the Vctrl node is about 6.3mV and the reference sidebands are only -21.87 dB relative to the center frequency.

According to figure 1, if the two loops are used, the voltage of the Vctrl node is shown in figure 7 when the PLL operates with the same conditions. Figure 8 is the enlarged partially of the figure 7. Figure 9 is the output spectrum of the frequency synthesizer. From figure 7-9, we can find that the voltage variation of the Vctrl node is about 1.28mV and the reference sidebands are -35.67 dB relative to the center frequency. So, the reduction of the reference sidebands of the proposed two loops architecture is 13.8dB more than that of the one loop. Also, the more the time constant of the integrator in figure 1 increases, the more the reference sidebands in PLL output reduce.

Figure 7. the transient voltage of the Vctrl node versus the locking time if the two loops are used

Figure 8. the enlarged partially of the figure 7

Figure 9. the output spectrum of the frequency synthesizer if the two loops are used
IV. CONCLUSION

An adaptive PLL frequency synthesizer architecture based on two loops is presented. One loop is for locking the PLL, and the other loop is for reducing the reference sidebands at the output of the frequency synthesizer. A 1.8V 1GHz frequency synthesizer is implemented in 0.18um CMOS process, and this design demonstrates that the proposed architecture can reduce the reference sidebands significantly.

REFERENCES


