Low Power Integrated Circuits for Wireless Neural Recording Applications

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Abstract - A group of prototype integrated circuits are presented for a wireless neural recording micro-system. An inductive link was built for transcutaneous wireless power transfer and data transmission. Power and data were transmitted by a pair of coils on a same carrier frequency. The integrated receiver circuitry was composed of a full-wave bridge rectifier, a voltage regulator, a date recovery circuit, a clock recovery circuit and a power detector. The amplifiers were designed with a limited bandwidth for neural signals acquisition. An integrated FM transmitter was used to transmit the extracted neural signals to external equipments. 16.5 mW power and 50 bps – 2.5 Kbps command data can be received over 1 MHz carrier within 10 mm. The total gain of 60 dB was obtained by the preamplifier and a main amplifier at 0.95Hz – 13.41 KHz with 0.215 mW power dissipation. The power consumption of the 100 MHz ASK transmitter is 0.374 mW. All the integrated circuits operated under a 3.3 V power supply except the voltage regulator.

I. INTRODUCTION

Simultaneous recording the activity of neurons is of great interest to neuroscientists and clinicians, which directly leads to the requirement of full implantable recording techniques [1]-[3]. Multi-channel microelectrode arrays with smart interface circuits offer a feasible approach for recording the responses of a single cell or a group ones [4]-[5]. This kind of hybrid devices even appears to be applied in human brain in the future as the signal acquisition module of the practical brain computer or machine interface (BCI or BMI) for the paralyzed patients.

A wide variety of neural recording microelectrodes have been previously reported [6]-[7]. However, most of these microelectrodes require direct wired connections to external equipment outside the body for transmitting the extracted signals from the neurons. In many medical applications, the connection with cables may result in the following three problems [8]-[11]: 1) an increase in the risk of infection; 2) a decrease in signal noise ratio; 3) hard to monitor the neural activity of unanaesthetized or freely moving animals. Therefore, signal transmission with cables is not suitable for chronic recording.

In this paper, we present an implantable micro-system. A group of prototype integrated circuits for bidirectional wireless telemetry and signal acquisition was introduced, which are capable of receiving power and command data from the outside circuits by inductive coupling, amplifying the neural signals and transmitting the results to external equipments. Section II introduces the architecture of the system. Section III describes the circuits for transcutaneous power and forward data transfer. The design of amplifiers for neural signal acquisition is given in Section IV. Section V presents an integrated 100 MHz ASK transmitter for reverse data transmission. The conclusions are drawn in section VI.

II. SYSTEM ARCHITECTURESE

Figure 1 shows the conceptual diagram of a wireless system for extracellular neural recording, which are composed of an implantable chip, an external circuit attached to skin and a computer that can be located several meters away.

The implantable chip will be integrated to a silicon-base microelectrode arrays as the interface between biological medium and external equipments. The power and command signals from the external circuit are recovered by the on-chip receiver module, and then be used to power and control the other implanted modules. The signal acquisition module is required by the implanted chip to amplify and digitalize the neural signals from one channel chosen from the multi-channel recording microelectrode arrays. After being encoded and configured by signal processing unit, the digitalized neural signals will be transmitted to outside through the RF reverse data transmitter with high data rate.

Due to the low coupling efficiency and high transmission attenuation, a bidirectional repeater link is built between the implanted chip and the host computer by a board-level circuit attached to skin (CATS). In uplink path, the commands from the computer is sent to an interface module on the CATS, and then be modulated to the carrier of power transfer. In downlink path, the extracted neural signals are received by CATS, and then sent to the host computer for further analyzing and processing. In addition, battery on CATS is

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used to power the circuit outside the skin and provide an adjusted power level to the implanted unit through an inductive coupling under the automatic feedback control from the implanted devices. The wireless recording system is designed to record extracellular neural activity of the animals with unrestricted movement.

III. TRANSCUTANEOUS WIRELESS POWER AND DATA TRANSFER

An integrated receiver circuitry was designed and fabricated, which consists of an on-chip full-wave bridge rectifier, a voltage regulator, a date recovery circuit, a clock recovery circuit and a power-level detector [12][13]. Three off-chip SMD capacitors are also necessary for coil resonant and voltage smoothing in implanted system, as is shown in Figure 1. Power and command data are transmitted through a single pair of coils using the same carrier frequency. The command data, which is used for selecting the recorded channel and adjusting the gain of the amplifier, can be recovered from the 1-10 MHz amplitude-modulated power waveform by data recovery circuit. Envelop detection method with a limited bandwidth is used for avoiding the low-frequency interference of the body moving or coils displacement. The frequency of the recovered clock signal is one half the frequency of the carrier. The current on the load of voltage regulator is sampled by the 4-level power level detector for feedback and automatic power control.

The performances of the internal receiver circuit are listed as follows:

1) Output voltage: 3.26 V
2) Dropout voltage: ≤ 40 mV (load=660 Ω)
3) Line regulation: ≤ 1 mV /V
4) DC Sensitivity (Input voltage range): 3.5 - 5.6 V
5) Regulator power dissipation: 220μA @ 3.5 V DC input
6) Frequency of recovered clock: 500 KHz @ 1 MHz
7) Data rate of command signal: 50 bps - 2.5 Kbps
8) Current thresholds for state changing: 5, 15, 25 mA

The power and reverse data receiver has been designed and fabricated in Hejian 0.18-μm CMOS 1P6M MS processing. Die micrograph is shown in Figure 2, and the chip area is 1.45 mm×1.35 mm.

IV. NEURAL SIGNAL AMPLIFIERS

Typical neural action potential signals from extracellular recording have frequency components in the range of 0.1 Hz - 10 KHz with amplitudes in range of 50 -500 μV[14]. As a result, amplification is needed before any further signal processing. The integrated amplifier proposed here is comprised of four parallel full-differential preamplifiers and a main amplifier. A 4:1 multiplexer selects channels to be amplified by the main amplifier. The generic block of the integrated neural signal amplifier is shown in Figure 3.
Figure 3. Generic block of the integrated neural signal amplifier

Figure 4. (a) Architecture of preamplifier and main amplifier (b) Schematic of OTA in preamplifier (c) Schematic of OTA in main amplifier

The architecture of the preamplifier and the main amplifier was originally proposed by Harrison in [15], which is shown in Figure 4(a). The mid-band gain $A_m$ is set by $C_1/C_2$ ($C_1, C_2>>C_n$), and the bandwidth is approximately $g_m/(A_mC_1)$, where $g_m$ is the transconductance of the operational transconductance amplifier (OTA).

In our design, a fully differential transconductance amplifier (OTA) with cascade topology is adopted by the preamplifier, as is shown in Figure 4(b). This structure reduces the sensitivity to supply and other noise so that good PSRR and noise performance can be obtained. Furthermore, a fully differential approach allows us to choose the value of output common-mode voltages accurately for optimum performance. The gain of this preamplifier is 20 dB. The fully differential structure is also adopted by the main amplifier. The two-stage topology transconductance amplifier provides high gain and high output swing, as is shown in Figure 4(c). The mid-band gain of the main amplifier is fixed at 40 dB.

Simulation results show that the integrated neural signal amplifier exhibits a gain of 60 dB from 0.95 Hz to 13.41 KHz with an input-referred noise of 4.92 μVrms. Under a 3.3 V supply, the power consumption of each preamplifier is only 7.5 μA and the main amplifier is 57.7 μA, which is 215 μW for each recording channel. The neural signal amplifier has been designed and fabricated in Chartered 0.35-μm CMOS 2P4M processing and it consumes about 2 mm² of chip area.

V. REVERSE DATA TRANSMITTER

An integrated reverse data transmitter [16], as shown in Figure 6, including a ring oscillator, a current-switch modulator, a band-gap current reference, a power transistor, and an off-chip antenna and a SMD capacitor are also necessary.

The transmitter is used to transmit the extracted neural signals to the outside equipments for further analyzing and processing in our neural recording system. A ring oscillator is used to generate the carrier waveform, which is modulated by the digital signal. Then the power transistor is driven by the modulated signal, and its output half-wave sinusoid current is radiated through the off-chip antenna.
amplifier was adopted to amplify the low-level neural signal composed of a four channel preamplifier array and a main power and forward data receiver. The integrated amplifier

2P4M CMOS processing. The command data (50 bps to 2.5 Kbps) and clock (500 KHz) can be recovered by an integrated power ASK transmitter can provide 100 MHz half-wave sinusoid current to drive the off-chip antenna with 0.374 mW power dissipation.

REFERENCES